

Docket No.: SNDK.344US0 Appln. No.: 10/796,575 Docket
Title: Flash Controller Cache Architecture

Inventors: Conley et al. Conf. No.: 1109 Group Art Unit: 2818 Filing Date: March 8, 2004 Arty. Tel: (415) 318-1160 Sheet 1 of 11

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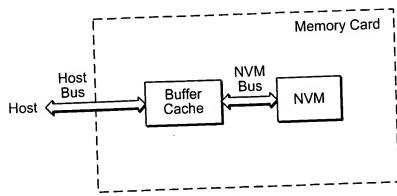


FIG.\_1(PRIOR ART)

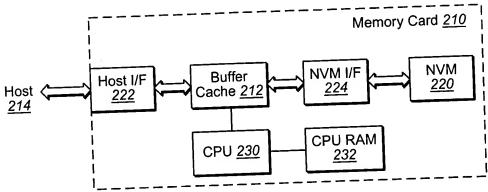


FIG.\_2

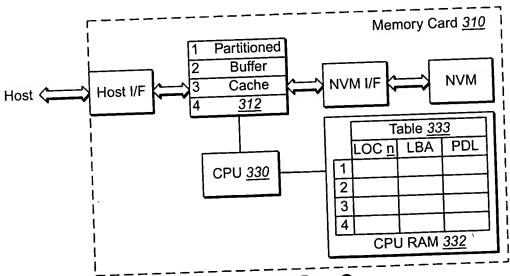
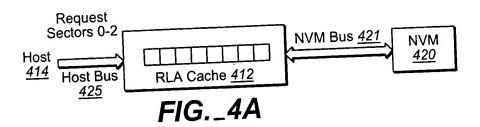
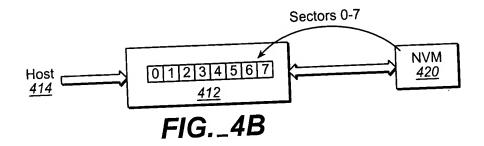
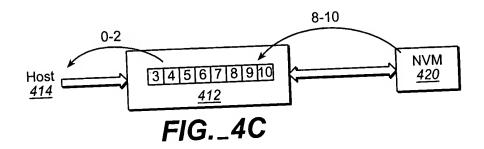


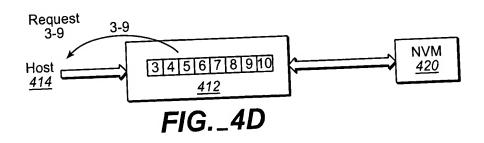
FIG.\_3

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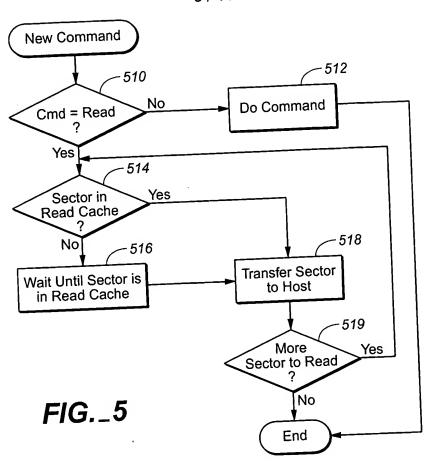


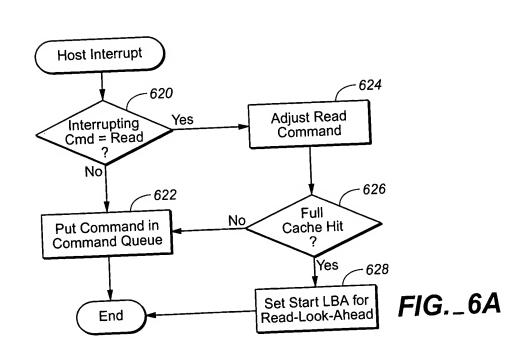


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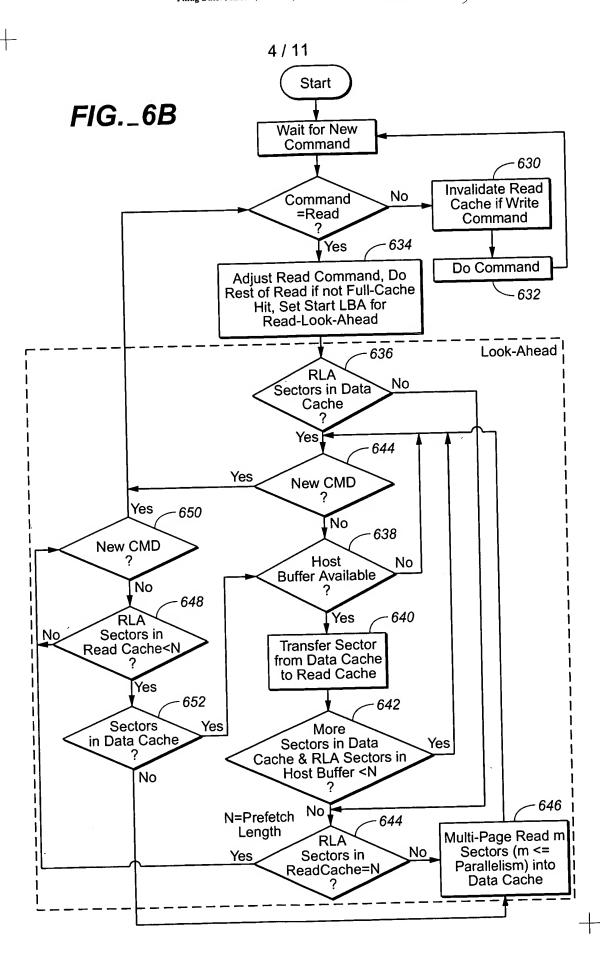
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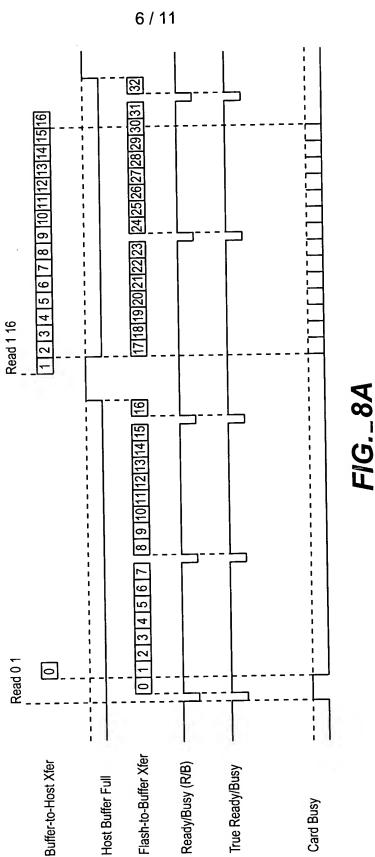
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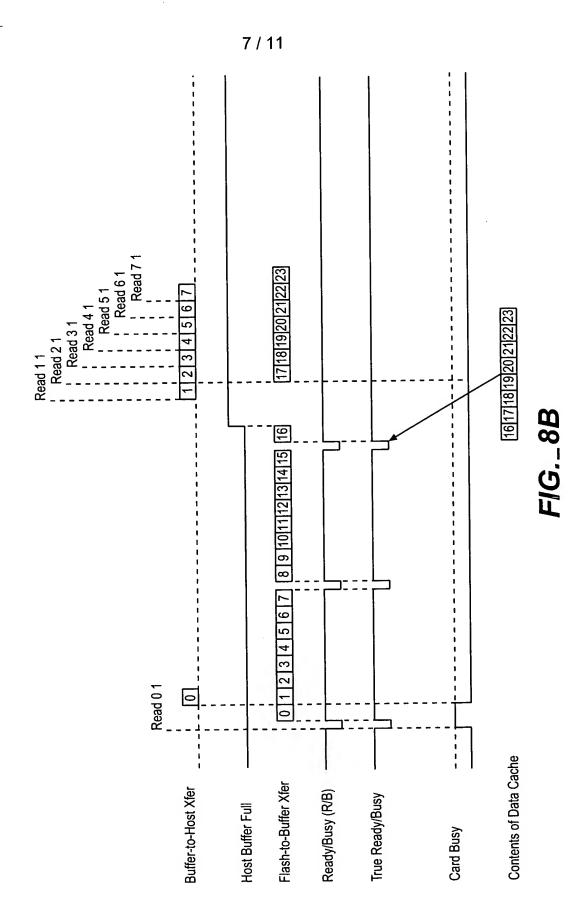
Buffer Cache (Host Buffer <u>707</u> Controller <u>705</u>	Cache Unit 0 Cache Unit 1 Current Cache Unit	
	Data Cache 11	
FIG7	Metapage X	
1 IG1	Flash <u>703</u>	
· · · · · · · · · · · · · · · · · · ·		

Cache Unit  Data Cache 01234567  Metapage X 01234567	Write Cache Unit 0 Write Cache Unit 1 Write Cache (Host Buffer) 0 1 2 3 4 5 6 7 Current Write		
FIG9 Metapage X 0 1 2 3 4 5 6 7	Controller		
riu9		Data Cache 01234567	
NVM 9 <u>09</u>	FIG9		

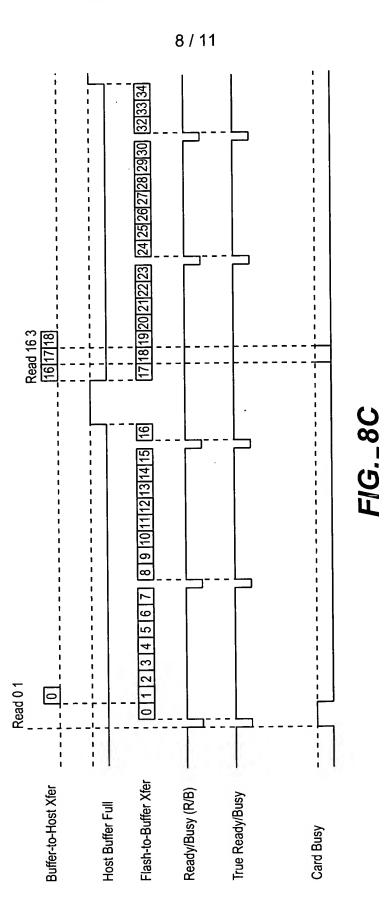
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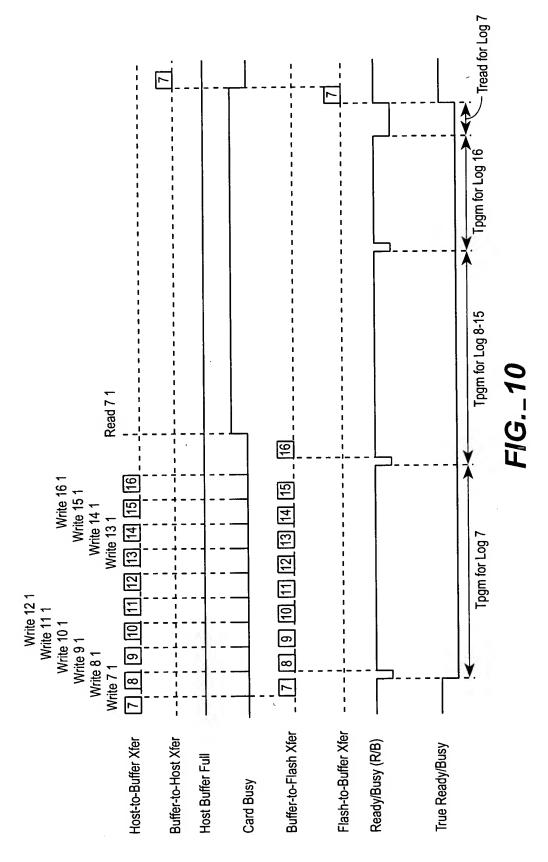


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